Performance analysis of different material based dual electrode doping-less TFET

Sunny Anand*, S. Inthekhab Amin, R.K. Sarin

Department of Electronics and communication Engineering, Dr. B. R. Ambedkar National Institute of Technology Jalandhar, Punjab, India

*Corresponding author: E-mail: sunnyanand.ec.13@nitj.ac.in

Received: 26 October 2016, Revised: 07 December 2016 and Accepted: 09 April 2017

DOI: 10.5185/amp.2017/607
www.vbripress.com/amp

Abstract

In this work, the charge plasma based dual electrode doping-less tunnel FETs (DEDLTFET) is simulated with the use of different materials such as silicon (Si-DEDLTFET), Silicon-germanium (SiGe-DEDLTFET) and SiGe at Source (SiGe Source DEDLTFET). The charge plasma technique is used to create source and drain region on an intrinsic body by selecting appropriate work function of metal electrode. The paper provides the comparison among devices on the basis of RF parameters. The on-state current (I_{ON}) for SiGe source DEDLTFET, SiGe-DEDLTFET and DEDLTFET are 1.84×10^{-4}, 8.75×10^{-5} and 8.11×10^{-6} A/µm respectively for similar off-state current (I_{OFF}). This result show that SiGe source DEDLTFET device provides better drive current along with improved ON-OFF current ratio (I_{ON}/I_{OFF}) and subthreshold slope (SS). Improved transconductance (g_m) and cut-off frequency (f_T) show that the hetero-material device has better RF performance while comparing with the other two devices. Copyright © 2017 VBRI Press.

Keywords: Charge plasma, band to band tunnelling (BTBT), sige hetero device, doping-less TFET (DLTFET).

Introduction

Due to nanometer technology, short channel effects (SCEs) have become a serious problem in metal oxide semiconductor field effect transistors (MOSFETs). To overcome different SCEs, one of the most proficient device is TFET [**1**], with properties viz. steep subthreshold swing (SS) and low leakage current (in OFF state). However, the concern for this device is low drive current under ON-state condition. Because of band-to-band-tunneling (BTBT) mechanism of electrons from source to channel [**2, 3**] the ON state current depends on the efficiency of BTBT. To increase the tunneling efficiency of TFET device, there are many techniques studied in the recent years [**2-4**]. Another challenge of TFET is to create uniform doping and form abrupt junctions for effective BTBT rate. The doping-less mechanism is the solution for the aforementioned problem, as source/drain regions are created with either charge plasma or electrostatic technique [**4-8**]. The fundamental principal of charge plasma based TFET is proposed in [**5**] and for enhanced analog performance is discussed in [**4**]. The reduction of ambipolarity of charge plasma TFET is thoroughly analyzed in literature [**7**]. The dopingless device can also be achieved through electrostatic doped technique [**8**].

In this work, we have proposed dual electrode doping-less TFET (DEDLTFET) [**4-5**] with the use of low band gap material (E_g) such as SiGe in the entire body instead of taking silicon material alone (SiGe-DEDLTFET) and SiGe at source region material only (SiGe Source DEDLTFET). The proposed device (SiGe Source DEDLTFET) utilize the wide band gap material silicon at channel and drain side, to achieve low OFF state current and source region is created using SiGe to increase the probability of tunneling. All the above-mentioned devices are not conventionally doped but the charge plasma technique is utilized to induce holes and electrons in source/drain regions [**6-7**]. For the same platinum and hafnium are used as source/drain electrode work function to induce charges of their respective concentrations in source and drain region. The paper also compares the RF performance of the proposed device with silicon based DEDLTFET (Si-DEDLTFET) [**4**] and SiGe DEDLTFET.

Device structures and parameters

The design of device structures and its characterizations are performed through TCAD ATLAS 2D [**13**]. The models used are, non-local band to band tunneling (BBT), Shockley- Read-Hall (SRH), constant voltage and temperature (CVT) mobility model. **Fig. 1** shows the device schematic of Si-DEDLTFET, SiGe-DEDLTFET and SiGe Source DEDLTFET. All the three transistors are considered with identical parameters such as silicon body thickness (t_{Si} = 10nm) and gate length (L_G = 50nm). Hafnium oxide (HfO_2) is taken as gate oxide material with a thickness of 3nm. The OFF state current in all the devices are kept fixed by considering a work function of 4.5 eV as gate metal electrode. The DEDLTFET is a doping-less device, where electrons and holes are induced by charge plasma technique [**7**] instead of using conventional doping. Platinum metal electrode (work function = 5.93eV) is used to form source region while hafnium metal electrode (work function = 4.4 eV) [**7**] is considered to form drain region. In SiGe-DEDLTFET and SiGe Source DEDLTFET, platinum metal electrode is used with a work function of 5.8eV to create 'p' source region. The mole fraction considered in this work is 0.5 [**9-10**]. The device structure parameters are listed in **Table 1.**

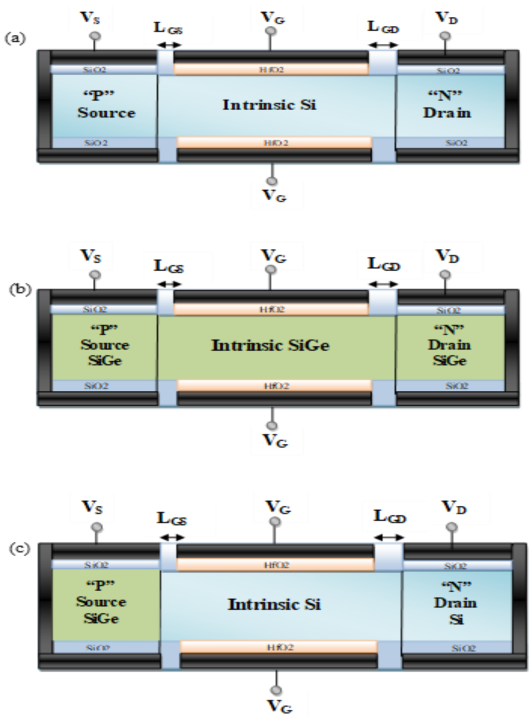

Fig. 1 Device structure of (a) Si-DEDLTFET, (b) SiGe DEDLTFET and (c) SiGe Source DEDLTFET.

Table 1. Parameters used for Si-DEDLTFET, SiGe-DEDLTFET and SiGe Source DEDLTFET.

Parameters	Si-DEDLTFET	SiGe-DEDLTFET	SiGe Source DEDLTFET
Gate Length (L_G)	50nm	50nm	50nm
Gate oxide	3nm (HfO_2)	3nm (HfO_2)	3nm (HfO_2)
Substrate material with thickness 10nm	Silicon	$Si_{0.5}Ge_{0.5}$	$Si_{0.5}Ge_{0.5}$:Source and Si: Drain
Gate Work Function	4.5eV	4.5eV	4.5eV
Channel Doping (n_i)	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}
Source Work Function	5.93eV	5.8eV	5.8eV
Drain Work Function	4.4eV	4.4eV	4.4eV

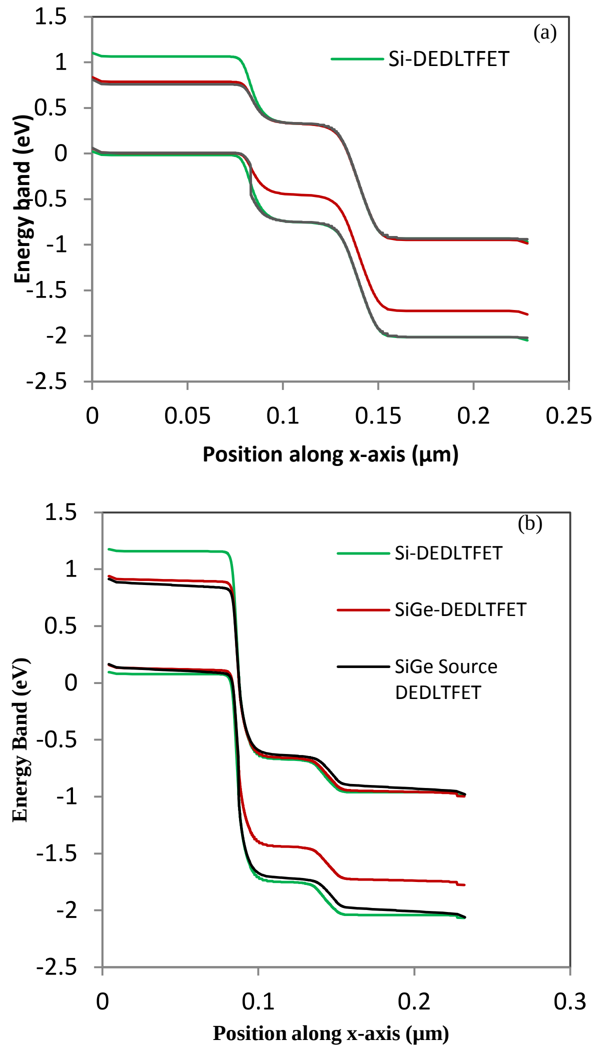

Fig. 2. Energy band diagram for Si-DEDLTFET, SiGe-DEDLTFET and SiGe Source DEDLTFET at (a) OFF state, (b) ON state.

Results and discussion

The energy band diagram in both OFF (V_{GS} = 0 V, V_{DS} = 1.0 V) and ON (V_{GS} = V_{DS} = 1.0 V) state is shown in **Fig. 2**, which gives the clarity about the design structure. The Si-DEDLTFET has constant band gap (E_g = 1.12eV) throughout the device and SiGe-DEDLTFET with E_g (= 0.67eV) as we have considered mole fraction x = 0.5. However for SiGe Source DEDLTFET, the SiGe is formed at source side only while silicon is at channel/drain region. Therefore, the energy band gap is different at source and channel/drain as shown in **Fig. 2(a)**. In On state condition, due to low bandgap of SiGe-DEDLTFET and SiGe Source DEDLTFET, the tunneling is high at source-channel region due to increased tunneling area as shown in **Fig. 2(b)**. As the result of it, probability of tunneling increases and hence drive current enhances. However in SiGe-DEDLTFET, the channel-drain tunneling rate is also high because of low E_g at channel and drain. This tends to increase reverse saturation current and hence performance degrades [**3**].

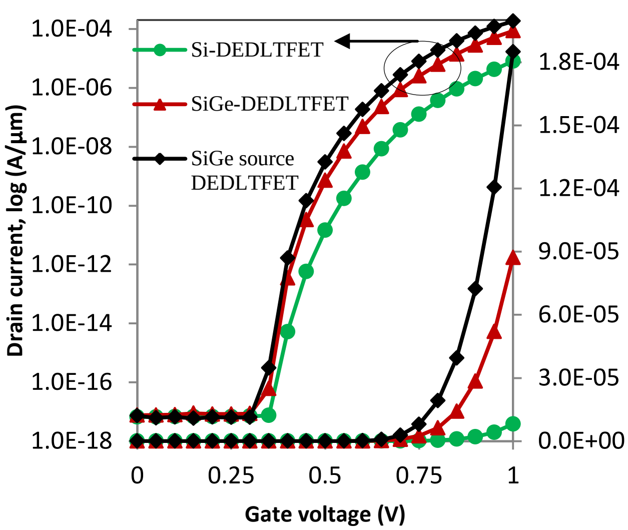

Fig. 3 Transfer characteristics (I_D-V_{GS}) for Si-DEDLTFET, SiGe-DEDLTFET and SiGe Source DEDLTFET at V_{DS} = 1.0 V.

Fig. 3 shows the plot of the transfer characteristics for Si-DEDLTFET, SiGe-DEDLTFET and SiGe Source DEDLTFET. While keeping the same off-state current for all the tree different configurations of devices, the ON-state current of the proposed device SiGe Source DEDLTFET clearly shows that by using SiGe at source only, provides better ON state current as compared to silicon (Si-DEDLTFET) and SiGe based TFETs (SiGe-DEDLTFET). The increase in ON state current is also attributed to increase in mobility. The SiGe material has higher mobility as compared to silicon. Moreover, these results can also be verified through the energy band diagram mentioned in **Fig. 2.**

With the use of low bandgap material at source region (SiGe) increases the tunneling probability (BTBT rate) and the use of wide band gap material (silicon) at channel/drain regions improves the leakage current (ambipolar conduction) [**7, 11**].

The transconductance is a very important parameter to analyse the cut-off frequency, the plot for the same has been shown in **Fig. 4** for all three devices. As g_m is directly proportional to the rate of change of drain current ($g_m = \partial I_D/\partial V_{GS}$) and the proposed device attains the maximum I_D for same biasing. Because of this reason the proposed device (SiGe Source DEDLTFET) possess better transconductance when compared to other two devices. The use of silicon germanium over the entire body, SiGe-DEDLTFET performance enhances as compared to silicon based device. Therefore, the increasing order of transconductance is Si-DEDLTFET <SiGe-DEDLTFET<SiGe Source DEDLTFET.

Fig. 5 shows gate bias dependency of total gate capacitances for all the three mentioned device configurations at V_{DS}=1.0V. The total gate capacitance ($C_{gg}=C_{gs} + C_{gd}$) is minimum for silicon based DEDLTFET throughout the gate bias, followed by SiGe Source and SiGe-DEDLTFET respectively. When compared with silicon, SiGe based devices have higher capacitance is because of higher electron concentration. The Cgg totally depends upon. Therefore, a SiGe Source DEDLTFET has higher gate to source capacitance and identical gate to drain voltage as compared to Si-DEDLTFET. As a result the total gate capacitance is higher for SiGe Source DEDLTFET. Similarly SiGe-DEDLTFET has higher total gate capacitance as compared to SiGe Source DEDLTFET.

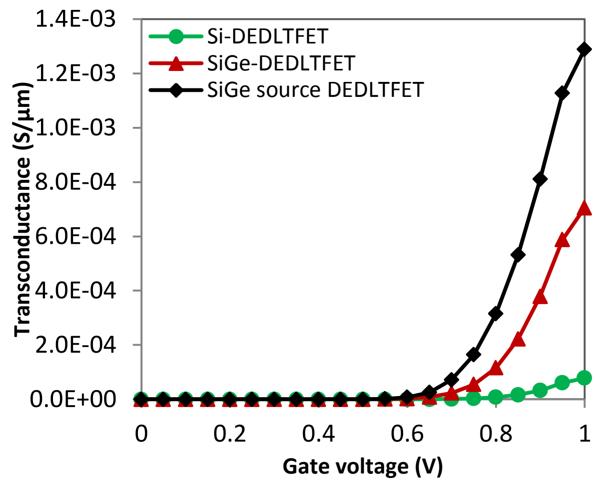

Fig. 4. Transconductance (g_m) performance for Si-DEDLTFET, SiGe-DEDLTFET and SiGe Source DEDLTFET at V_{DS} = 1.0 V.

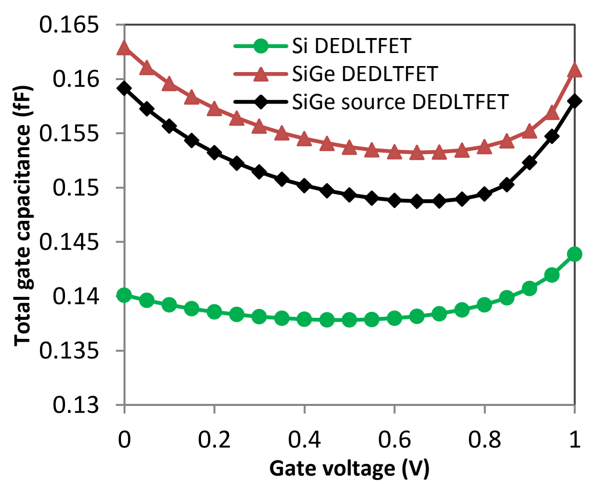

Fig. 5 Total gate capacitance (C_{gg}) for Si-DEDLTFET, SiGe-DEDLTFET and SiGe Source DEDLTFET with respect to gate voltage at V_{DS} = 1.0 V.

The unity gain cut off frequency ($f_T = g_m/2\pi c_{gg}$) for Si-DEDLTFET, SiGe-DEDLTFET and SiGe Source DEDLTFET at constant drain bias (V_{DS} = 1.0 V) is shown in **Fig. 6**. As f_T depends upon transconductance and total gate capacitance, the deviation in value of C_{gg} for all three devices do not show much variation (in femto farad), so dependency of f_T is totally based on g_m. Therefore, SiGe Source DEDLTFET provides maximum cut-off frequency as transconductance is maximum for the same as shown in **Fig. 4.** The g_m is minimum for Si-DEDLTEFT and because of that f_T is also minimum as compared to for SiGe-DEDLTFET.

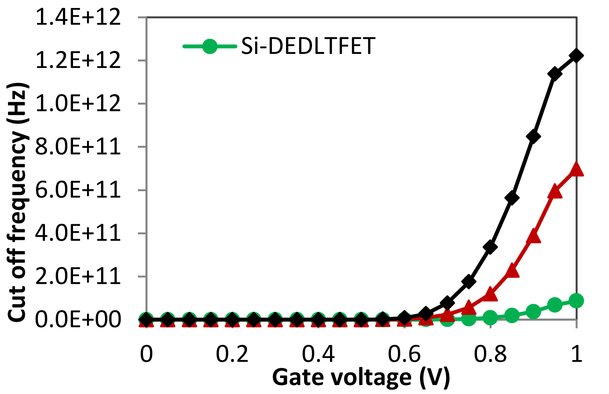

Fig. 6 Cut-off frequency (f_T) for Si-DEDLTFET, SiGe-DEDLTFET and SiGe Source DEDLTFET with respect to gate voltage at V_{DS} = 1.0 V.

Table. 2 shows a brief comparison of the proposed device with few available recent literatures. The proposed device show far superior Ion with improved I_{ON}/I_{OFF} ratio. The steep average subthreshold (SS_{av}) helps the device to have better switching performance for digital circuit applications.

Table 2. Comparison of different doping-less TFETs.

Reference	I_{ON} (mA/µm)	I_{ON}/I_{OFF}	SS_{av} (mV/decade)
Kumar *et al.* [**5**]	~ 4×10^{-7}	1.1×10^{12}	~ 100
Anand *et al.* [**4**]	~ 1.8×10^{-5}	6×10^{12}	~ 55
Bashir *et al.* [**12**]	~ 4×10^{-5}	5×10^{12}	~ 38
This work	1.85×10^{-4}	2.5×10^{13}	~ 23

Conclusion

In this work, with the help of extensive study, we have demonstrated the performance enhancement of proposed device SiGe Source DEDLTFET. The use of SiGe at source side in DEDLTFET results in the reduction in band gap and narrowing of band helps to improve tunneling rate. The reduction in tunneling width helps to enhance the ON-state current and increase the steepness for better switching. The device is further investigated for RF parameters such as transconductance, capacitance and cut-off frequency. A comparative analysis has been done with Si-DEDLTFET and SiGe-DEDLTFET. The SiGe Source DEDLTFET is found to have improved drain current, transconductance, and unity gain cut-off frequency. Through simulated results it is concluded that SiGe Source DEDLTFET provides better RF performance as compared to the other two mentioned device structures.

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