Evolution of the performance of SiNWs based electrochemical capacitor in ionic electrolyte

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Abstract

The development of micro-supercapacitor (µ-SC) based on silicon nanowires (SiNWs) has increased the demands of cost-effective methods via low temperature processing routes for the fabrication of SiNWs which can enable the realization of µ-SC directly on a Si chip. In this work, SiNWs synthesized by hot-wire chemical vapor processing (HWCVP) at low substrate temperature of 350 ^{o}C have been explored as the electrodes for the use in µ-SC. Electrochemical behavior was tested by using cyclic voltammetry (CV) and galvanostatic charging/discharging in an ionic electrolyte. TEM characterization reveals as-grown SiNWs have inner crystalline core (c-core) sheeted with an amorphous layer of silicon (a-Si) which has poor electrical conductivity and reduces the capacitance of SiNWs. Copyright © 2017 VBRI Press.

Keywords: VLS mechanism, silicon nanowires, hot-wire CVP, micro-supercapacitor, cyclic voltammetry.

Introduction

In the recent years, researchers have been making great efforts to have an on-chip energy source in order to make devices more compact and portable to meet the present demands of miniaturization **[1-4]**. Micro battery has been successfully tested for on-chip application but it does not meet the requirement of long term usage and has complex structure as it has two different electrode materials **[5]**. Further, the electrode material in battery is not compatible with micro-electro-mechanical system (MEMS) technology. Silicon on the other hand being compatible with MEMS technology is widely investigated as an anode material for lithium ion battery **[6]**. However, cycle stability of Si based battery is a big issue due to large volume change of Si anode during charging and discharging. In order to overcome these issues, the supercapacitor may serve as an alternative to the battery because of its long life, ease of fabrication (due to its simple geometry as both the electrodes are of the same material) and absence of hazardous chemicals **[7]**. As the batteries and fuel cells are restricted in terms of power density, supercapacitor can also be combined with the respective devices to overcome this challenge. Carbon based materials such as porous carbon, carbon nanotubes (CNTs), graphene and carbide-derived carbon have been shown great performance for the application in supercapacitors **[8-11]**. But the integration of these materials into MEMS requires high temperature routs and multiple complex steps. Moreover, these materials are not fully compatible with the standard Si chip technology. In order to resolve these issues, an electrode material is needed which must be compatible and scalable to meet MEMS requirements. In this context, SiNWs having high surface area, reproducibility, compatibility and scalability with the MEMS can be a promising candidate for µ-SC application. Moreover, their size and doping level can be varied by adjusting the growth parameters, which consequently can control the capacitance of SiNWs based µ-SC.

J. W. Choi *et al.* have demonstrated the use of the porous SiNWs in supercapacitor and these SiNWs showed a stable capacitance at high current density as compared to porous carbon **[12]**. Later on, F. Thissandier and co-workers **[13, 14]** have reported results of a study on SiNWs as electrodes in µ-SC with the value of specific capacitance in the ranges of 20-440 µF/cm^2. However, these studies require high processing temperature to synthesize SiNWs in thermal CVD. To solve this issue, SiNWs were also fabricated directly on a silicon wafer by chemical etching process **[15, 16]**. In that process fabrication of two electrodes of a µ-SC on a Si substrate is very difficult. Moreover, this method is limited to a particular Si substrate and cannot be extended for flexible low cost polymer substrate which is the demand of future flexible devices **[17-19]**. It is therefore necessary to develop the SiNWs based µ-SC by a simple and low temperature process. Alternatively, economical and well-defined SiNWs synthesized at low temperature 350 ^{o}C via VLS mechanism by HWCVP technique may offer a great opportunity as µ-SC electrodes for various applications

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including implantable medical devices and flexible electronics **[20, 21]**.

In the present work, SiNWs were synthesized by HWCVP technique which enables the growth at a substrate temperature of 350 ^{o}C. Such low temperature for the growth of SiNWs makes the process viable for direct fabrication of µ-SC on a chip and also reduces the cost of material production. After the growth of SiNWs their capacitor performance was evaluated by cyclic voltammetry and galvanostatic charging/discharging curves.

Experimental

SiNWs were grown on Stainless steel (SS 316) substrate by HWCVP technique via Vapor-Liquid-Solid (VLS) mechanism using Sn as a catalyst **[22, 23]**. **Fig. 1** illustrates the process steps which are involved in the growth of SiNWs. Before loading into the deposition chamber the substrate was cleaned using ultra sonication in methanol for five minutes. A thin film of Sn was deposited on the substrate by thermal evaporation of Sn powder. This Sn film was treated with atomic hydrogen which was generated by a heated Tantalum filament in the HWCVP chamber in order to form the Sn nano-template **[22]**. The substrate temperature was fixed at 350 ^{o}C. Synthesis of SiNWs was then done on the prepared Sn nano-template by passing SiH_4 gas over the heated filament at 1700 ^{o}C temperature and at substrate temperature of 350 °C. After that, µ-SC was fabricated in two electrodes configuration comprising of two identical SiNWs electrodes. Filter paper dipped in the ionic electrolyte 1-Ethyl-3-Methylimidazoliumbis imide was used as a separator between the two electrodes. Scanning electron microscopy (SEM, Jeol, JSM-7600F) and X-ray diffraction were employed in order to obtain the information regarding morphology and crystalline structure of SiNWs, respectively. Their crystal structure was also studied by Transmission electron microscopy (TEM, Jeol, JEM 2100F) and Raman spectroscopy (Horiba, HR 8000, Argon laser 514.5 nm). Bio- Logic system (Model, SP-300) was used to evaluate the electrochemical performance of SiNWs.

Results and discussion

Fig. 2 depicts SEM images of morphology of the used Sn nano-template for the growth of SiNWs and the as-grown SiNWs. This image shows that the HWCVP grown SiNWs are tapered. The diameter of SiNWs was determined in the range of 100-150 nm. On the other hand, the size of the catalyst particles is found in the order of 20-50 nm.

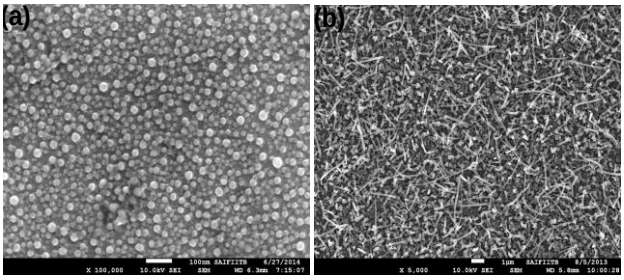

Fig. 2. (a) FEG-SEM image showing the morphology of Sn nano-particles and (b) the as-grown SiNWs.

According to VLS mechanism the diameter of the resulted SiNWs should be equal or smaller than the used template size **[24]**. The above statement could not be validated over here because of the radial growth of amorphous Si film on SiNWs during the growth. It can be seen that the diameter of the resulted SiNWs (100-150 nm) is much larger than the used nano-template size (20-50 nm). It is also observed over here that the diameter decreases towards the end of SiNWs which is due to the radial deposition of Si **[25]**. The presence of amorphous coating of Si is confirmed by Raman spectroscopy as depicted in **Fig. 3 (a)** which consists of a broadband peak at 480 cm^{-1} attributing to the amorphous part. In addition, a sharp peak at 520 cm^{-1} is also assigned which is due to the scattering of light by the crystalline core. Therefore, SiNWs synthesized by HWCVP have an amorphous coating of Si on c-core. SiNWs sample was also characterized by the X-ray diffraction to identify the crystalline phase present in SiNWs. XRD analysis confirms the phase of silicon and crystalline nature of

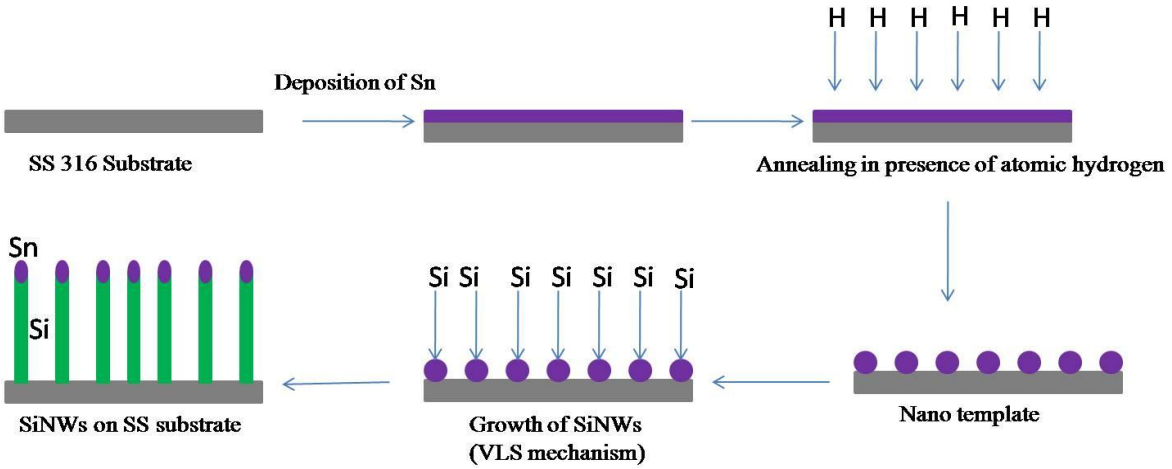

Fig. 1. Systematic representation of the steps involved in the growth of SiNWs via VLS mechanism.

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SiNWs (**Fig. 3 (b)**). XRD result shows crystalline peaks of (111) and (311) which have been identified by determining their position in XRD spectrum. Rest of the peaks may be attributed to the scattering of X-rays from the substrate.

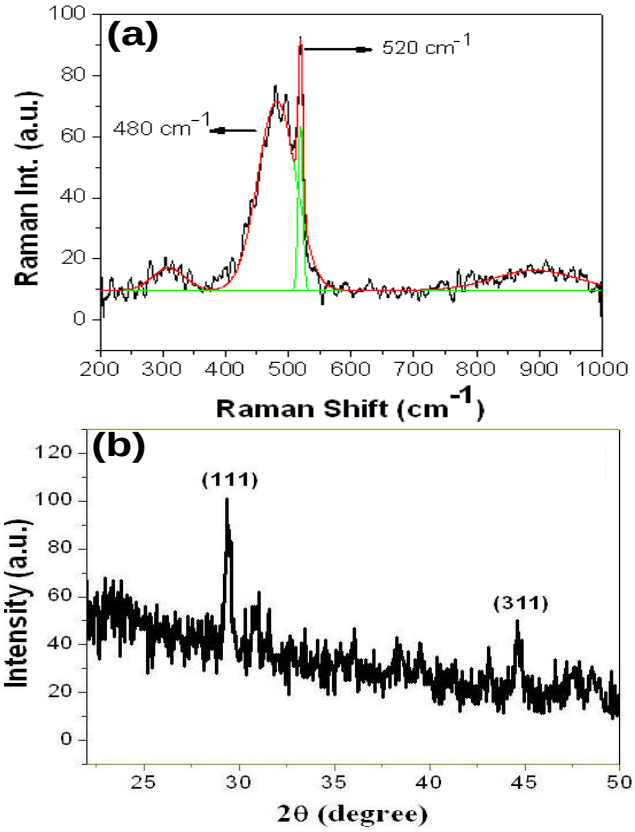

Fig. 3. (a) Raman spectra and (b) XRD pattern of SiNWs grown by HWCVP.

It can also be seen in HR-TEM image (**Fig. 4)** that the diameter of the c-core of SiNWs is 20-25 nm which is nearly same to the size of the used template, confirming that the growth of c-core occurs via VLS mechanism. The d spacing for the c-core is determined to be 0.31 nm which stands for [111] growth direction of SiNWs. The size of the crystalline core is decided by the size of the used Sn particles size whereas the thickness of the a-shell is proportional to the growth duration and increases with the growth duration.

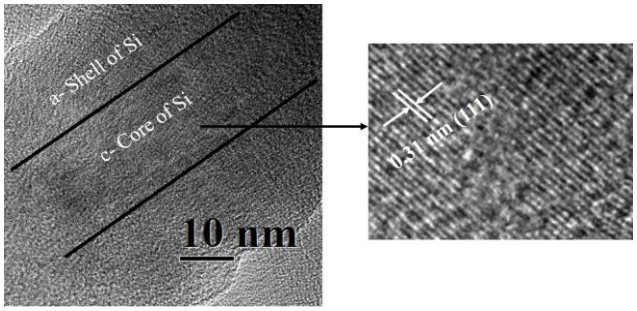

Fig. 4. HR-TEM image of a single SiNW, which shows that SiNWs consist of two regions, a-Si shell and c-Si core. The enlarged image exhibits periodic arrangement of Si atoms in the c-core.

To study their capacitive behavior, CV was performed between voltages 0-1.3 V at different scan rates of 40, 60, 100 mV/sec as shown in **Fig. 5 (a)**. For an ideal capacitor, a rectangular shape of CV curve is expected and as we see that the shape of CV curves is about quasi rectangular indicating nearly capacitor characteristics of SiNWs. After CV measurement, SiNWs based capacitor was charged/discharged in a constant current mode between the voltage of 0- 1.3 V. During charging and discharging the current was maintained at a constant value of 50 µA. The observed charge/discharge behavior of SiNWs is plotted in **Fig. 5 (b)**.

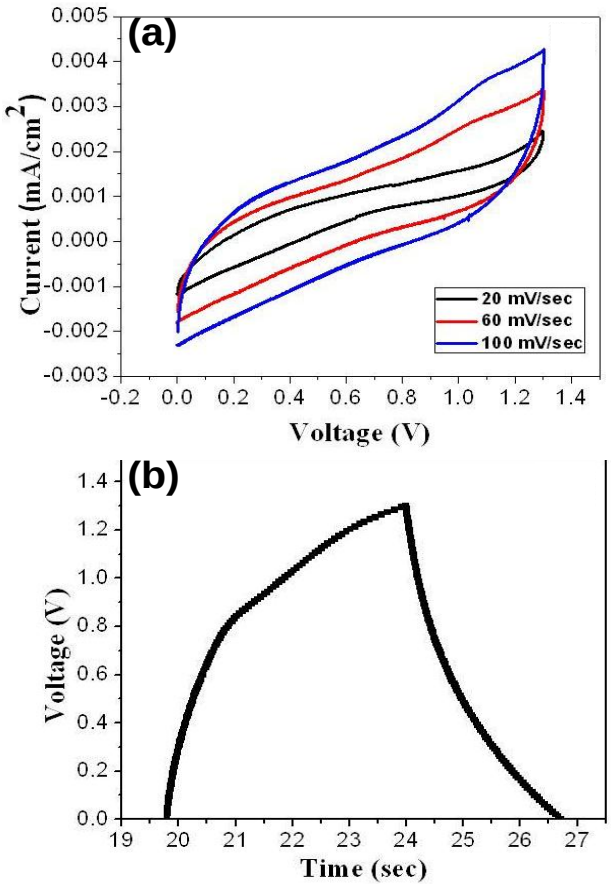

Fig. 5. (a) CV curves and (b) charging and discharging curves for SiNWs based capacitor.

It can be seen from the charging/discharging curves that the voltage has almost linear relationship with the time and the voltage behavior is symmetric in charging and discharging state showing the characteristics of a capacitor. The voltage ranges on a capacitor is decided by the used electrolyte in the capacitor. For SiNWs, in this particular ionic electrolyte the maximum voltage limit is determined to be 1.3 V. SiNWs capacitance is calculated with the help of following equation:

$$C = 2\left(\frac{(I_+ + I_-)/2}{v \times A}\right)$$

where, C is the capacitance per unit are, v is the scan rate, I_+ and I_- are the currents measured during charging and discharging states and A is the electrodes area. The value

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of C is the average of the capacitance calculated at different voltage point in the CV curve. The specific capacitance calculated by the CV curves is about 21 μF/cm^2 at the scan rate of 40 mV/sec. However, this value is lower than the reported value of SiNWs based μ-SC in literature **[13, 15]**. In that study SiNWs were grown by thermal CVD process or by wet chemical etching of wafer which give crystalline wires free from any amorphous phase.

HWCVP grown SiNWs have a-shell and c-core structure. Therefore, there are two factors with SiNWs based electrodes, wire length and the amorphous coating of Si, which are responsible for overall change in the capacitance value. Length is responsible to enhance the capacitance whereas the radial a-Si coating works as a reducer to the capacitance because of its poor electrical conductivity (~ 10^{-8} S/cm).

Conclusion

SiNWs grown by HWCVP are investigated for the use in μ-SC. The amorphous shell on SiNWs plays a vital role in determining the capacitor performance and its thickness should be minimized as much as possible in order to increase the overall electrical conductivity of SiNWs. HWCVP grown SiNWs showed a capacitance of 21 μF/cm^2. Further improvement is possible by removing the a-Si coating completely by using atomic hydrogen or by depositing a conducting layer on them. It is believed that this structure may be suitable for fabricating μ-SC in MEMS technology. These SiNWs are also suitable for prospective flexible electronics applications such as μ-SC on flexible substrates and wearable electronics.

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