REVIEW ARTICLE

Know-how needs for Higher Education in Nano-electronics: French CNFM Network Strategy

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Microelectronic technologies have progressively shifted to nanotechnologies thanks to a permanent decrease in the size of elementary devices over the last 50 years. This evolution has been achieved by decreasing the lateral dimensions of the devices, and the thicknesses of the layers involved in the architecture of the devices. The minimum dimensions have today reached the size of several atoms. New concepts are introduced to better control the fabrication processes and, therefore, the electrical properties of circuits and systems. In parallel, the application spectrum of microelectronics has been broadened, which allows developing complete integrated systems such as connected objects, which also broadens the necessary skills of designers in a multidisciplinary manner. Research and industry therefore have a strong need for such skills and competences. As a consequence, Higher education must continuously adapt to meet these needs. This approach requires the existence of technological platforms, which are becoming more and more expensive due to the increasing complexity of the technology and which must be shared. In France, a national network was created and organized in this way. Based on several examples of the activities of the French common centers, this paper presents how to maintain a high scientific level and skills based on the knowledge and know-how of future engineers and researchers.

Introduction

Microelectronic technologies have gradually shifted towards nanotechnologies thanks to a permanent decrease in the size of elementary devices over the past 50 years. This evolution has been achieved by reducing the lateral dimensions of the devices, and the thicknesses of the layers involved in the architecture of the devices [**1**]. The minimum dimensions have now reached the size of several atoms [**2**]. New concepts applying quantum physics, low energy consumption and new processes, mainly at low temperatures to minimize diffusion mechanisms, have been developed in addition to traditional microelectronic technologies [**3**]. New materials such as graphene [**4**], carbon nanotubes, silicon nanowires [**5-7**] and very thin films [**8**] have been introduced to better control manufacturing processes and thus the electrical properties of circuits and systems [**9**]. The new integration increasingly involves the third dimension by stacking at the level of the integrated circuit the channel of nanowires [**10**], or by stacking the dies in order which has led to new packaging techniques at the nanoscale [**11**].

At the same time, the application spectrum of microelectronics has broadened, making it possible today to develop complete integrated systems such as connected objects that require a combination of several electronic functions but also sensors, actuators and communication modules. These objects represent the challenge of the next ten years, as evidenced by numerous studies [**12, 13**].

Research and industry therefore have a great need for these skills and competences.

These qualities require a strong knowledge but also a mandatory know-how. Without know-how, the skills are mainly virtual and too far from the control of physical objects. Higher education in this field must make an effort to provide these skills to future engineers and PhD students, but also to industry employees in the context of lifelong learning [**14**].

In the field of nanotechnologies, knowledge acquisition is the result of research [**15**]. **Fig. 1** shows the cycle that allows the development of practical training in initial training at the master's and engineering levels (before the doctorate). It is clear that know-how is the key to innovation and allows a return to research and development after graduation.

This practice training requires the existence of platforms for design, modelling, manufacturing and testing, which are becoming increasingly expensive due to the very high accuracy required.

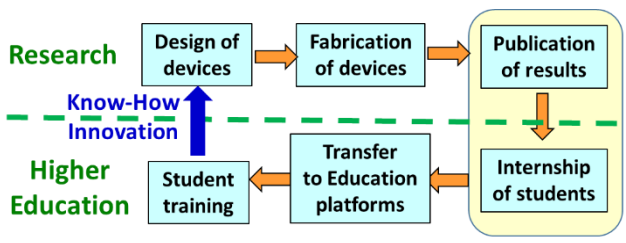

Fig. 1. Schematic cycle from researchers to new researchers through initial education. At the level of Higher Education, research and teaching are strongly interdependent [**15**].

The French National Network of Microelectronics and Nanotechnologies (CNFM) was founded with the aim of creating common inter-university centers including platforms of practice in computer-aided design, manufacturing, characterization and testing dedicated to higher education [**16**].

Thus, this article deliberately addresses the need for know-how in the context of microelectronics and nanotechnologies with the organization of the educational structure capable of providing future graduate engineers and masters with the skills and competencies by preparing them for research and development activities, a mandatory need for research laboratories and companies in the field.

Fig. 2 schematically shows the goal and the structure of the paper.

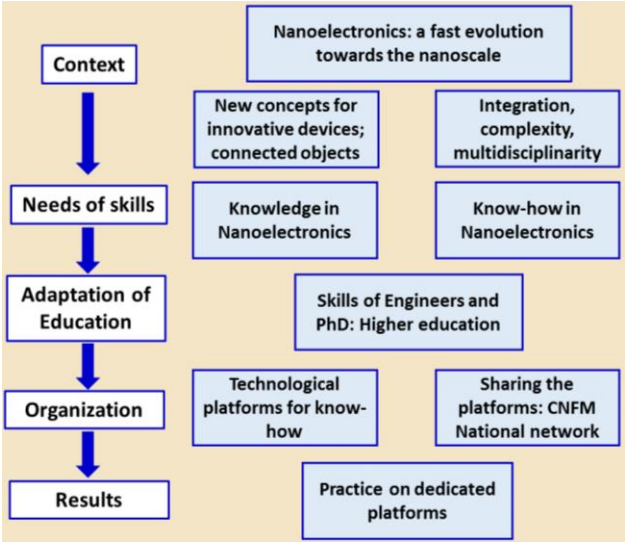

Fig. 2. Simplified flowchart of the content of the article: from the context of the very fast evolution of the microelectronics and nanoelectronics field, to the associated skills and know-how and the related practice training performed on dedicated platforms.

After a presentation of the context, the needs of skills and know-how is highlighted. The French organization able to answer to this demand is then described in order to understand its capabilities to offer to student the best conditions of learning. Then, several examples of the practice training relating more particularly to devices based on nanowires, graphene films and quantum dots will be detailed. It is obvious that all these practices result from research activities. Let us notice that this transfer from research to higher education requires a relative long time that explains the delay between the first research results and the final practice in the curricula of students.

Evolution of the microelectronics technologies

Reduction of the lateral dimensions on elementary devices

Microelectronics technologies have progressively shifted to nanotechnologies thanks to a permanent decrease in the size of elementary devices over the last 50 years. This evolution has been achieved by decreasing the lateral dimensions of the devices, and the thicknesses of the layers involved in the architecture of the devices [**1**]. The minimum dimensions have today reached the size of several atoms. **Fig. 3** shows the evolution of the channel length of a MOSFET (Metal-Oxide-Semiconductor Field Effect transistor) that is a significant geometrical parameter of an electronic device. The channel length has decreased from several microns to several nanometers all along the last thirty years.

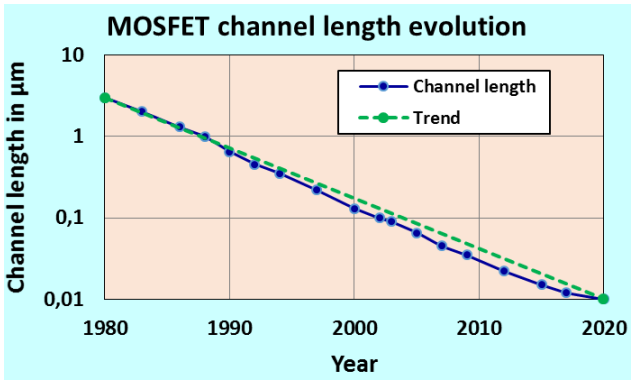

Fig. 3. Simplified flowchart of the content of the article: from the context of the very fast evolution of the microelectronics and nanoelectronics field to the associated skills and know-how and the related practice training performed on dedicated platforms.

This geometrical reduction of minimum size has led to an improvement of the integration capabilities. The Moore's law proposed by G. Moore in 1965 [**1**] reflects this evolution, which has been exponential over the past fifty years.

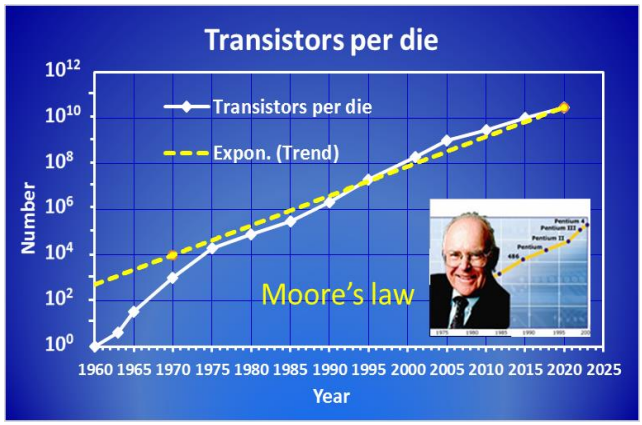

Fig. 4. Moore's Law: Proposed in 1965 [1], this heuristic predict the evolution of the integration with an exponential growth.

New concepts applying quantum physics, low energy consumption and new manufacturing processes mainly at low temperatures to minimize diffusion mechanisms have been developed in addition to traditional microelectronics technologies. New materials such as graphene [**4**] are being introduced to better control manufacturing processes and, consequently, the electrical properties of circuits and systems [**2**].

Nanoscale and new nano-devices concepts

New integration increasingly involves the third dimension by stacking integrated circuit chips, which has led to new packaging techniques at the nanoscale. At the same time, the application spectrum of microelectronics has been broadened by micromechanical and optical processes, which now makes it possible to develop complete integrated systems such as connected objects [**17**]. These objects may contain sensors, actuators, communication modules, and signal processing functions [**18**].

Fig. 5 shows the new evolution that takes into account the introduction of new technologies, the third dimension and even more so the notion of systems such as System on Chip (SoC) and System in Package (SiP) [**2**]. In comparison with Moore's Law, the integration of functions up to 100,000 components (right vertical scale) can lead to an equivalent density of elementary devices 100 times higher than that of conventional integrated circuits (left vertical scale).

Fig. 5. More than Moore's Law. Since 1995, the integration concerns systems that may contain millions of transistors each. The average density of elementary devices can be multiplied by one hundred (*After* M. Swaminthan *et al*. [**2**]).

This evolution is linked to the incredible improvement of the technological process steps and of the associated design tools involved in the CAD (Computer-Aided-Design). Heterogeneous system can be designed and fabricated nowadays, such as connected objects, included in the Internet of Things (IoT).

As shown in **Fig. 6**, the architecture of the connected object includes sensors and actuators, signal processing, energy harvesting, transmission and reception circuits based on communication protocols, as well as monitoring systems and the corresponding control and monitoring ergonomics [**17**].

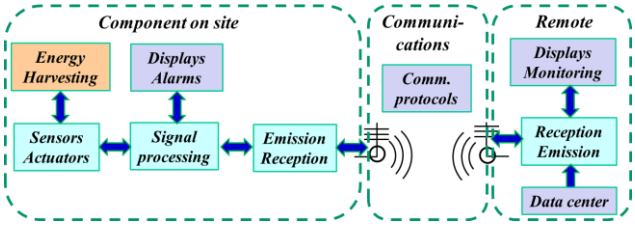

Fig. 6. Schematic architecture of a connected object. Several functions are integrated [**17**].

Sensors and actuators can be mechanical, optical, chemical and biological, which also broadens the necessary skill domain of engineers and designers in a multidisciplinary manner [**18**].

The development of connected objects is huge. **Fig. 7** shows the expected growth of their production during the next ten years. This survey takes into account all the objects that are presently connected, including iPad, cellular phones and all the other applications to health, transport, security, environment, energy, etc. [**17**]. The growth is exponential, similarly to the Moore's Law.

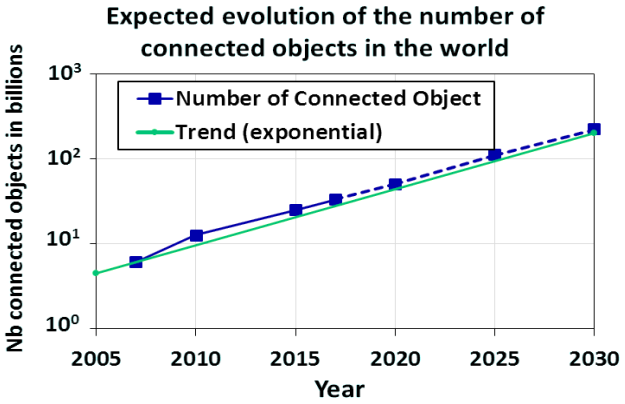

Fig. 7. Expected evolution of the number of connected objects from 2018 to 2030 [17].

It is clear that such an evolution requires human resources in technicians, scientists, engineers and doctors. These future employees must be prepared for their future missions including innovative approach [**19**], which include the permanent increase of integration while meeting the new challenges of developing heterogeneous systems for connected objects and reducing their energy consumption.

Global view of higher education in nanoelectronics

The training of specialists in electronics, microelectronics and nanoelectronics is increasingly using online tools such as MOOCs [**20,21**]. Education systems are therefore increasingly keen on these tools, since they suggest that the cost of training engineers, technicians or doctors will be significantly reduced by reducing the number of teaching staff. It appears that with the fabulous increase in complexity, graduates increasingly need to master theoretical knowledge through exercises, problem-based learning or flipped classes, but most of all practical training on equipment and tools and therefore to acquire know-how [**22**]. Due to the increasing cost of these equipment and tools, it is increasingly difficult for an academic institution to have access to the entire design, manufacturing, characterization and testing chain of components and systems in the field of nanotechnology. Even in world-class universities, very few students, even at the doctoral level, are allowed to carry out a cleanroom manufacturing process on their own. In order to correct this trend, it appeared that a pooling of equipment and tools between several institutions and within the

framework of a national network allowed future graduates to have experience of know-how both on design software and on technological process modules or characterization benches. It is in this educational strategy and with a view to meeting the needs of industries and research and development centers that the French national network dedicated to the training of high-level specialists in microelectronics and nanotechnology was created in the early 1980s [**23,24**].

Organization of the French national network

The French national network of microelectronics and nanotechnologies (CNFM) was set-up with the aim of creating joint interuniversity centers that include platforms of practice in computer-aided design, manufacturing, characterization and testing. This network has an official structure (Public-Interest-Group) recognized by the Ministry of Higher Education and entitled with the acronym GIP-CNFM [**16**]. It is composed of twelve interuniversity centers (**Fig. 8**) that are all attached to an academic institution, and of two industrial bodies.

The industrial body of the companies of the field of electronics and microelectronics, "ACSIEL Alliance Electronique", represents more than 160 companies that have activities in France [**25**].

As shown in **Fig. 8**, the twelve centers are now operational and offer access to more than eighty technical platforms, including seven clean rooms [**16**].

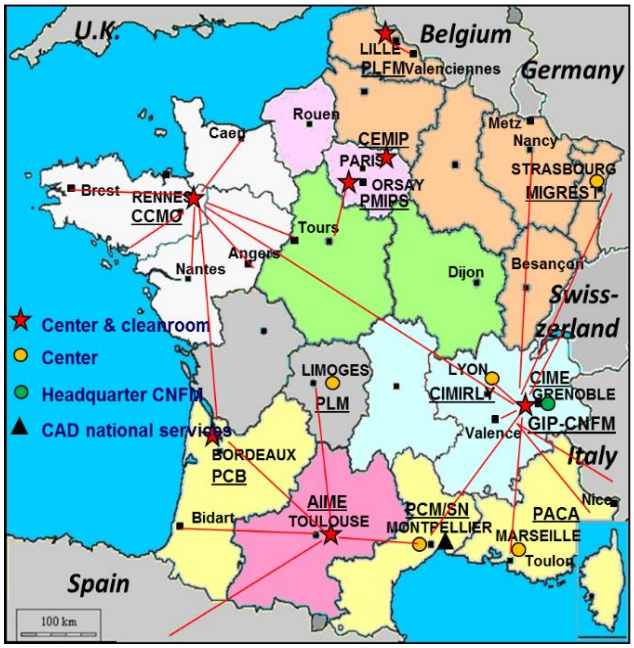

Fig. 8. Geographic distribution of the CNFM centers (National Coordination for Education in Microelectronics and nanotechnologies). The 12 centers share the platforms with the regional institutions [16,24].

Fig. 9 shows the key figures of the network for the last academic year. During this academic year, more than 16,000 students from 89 French academic institutions and 60 research laboratories used the network and received training on the platforms.

These platforms are used for initial education devoted to the basic know-how, for example the design, the fabrication, and the characterization of a silicon based diodes or NMOS transistors. Students in initial training spend an average of one week of cleanroom practice and five weeks of characterization, testing and CAD. Because the cost to create and maintain the platforms is very high, several equipment are shared not only with several institutions for education purpose, but also with several research laboratories. About 1,250 PhD students and their advisers are users of these platforms.

12 CNFM interuniversity centers and 2 industrial bodies (ACSIEL, FIEEC)

81 platforms among them 7 cleanrooms (100 M€ total invest)

Budget: 1M€ ➔ induced 21M€

National CAD services for testing, software's, prototyping

16,000 students/year (1,250 PhD)
830,000 hours*students/year

The users:
- **89 Higher education institutions**
- **60 research laboratories**
- **many companies**

Fig. 9. Key figures of the CNFM network. More than 16,000 students are users of the platforms each year. About one fifth are trained on nanotechnologies platforms [16].

But the mission is also to prepare students for the future, and an innovation strategy was initiated in 2010, with new practices adapted to the expected future technologies. The GIP-CNFM network has successfully applied for two national innovation programs, the first entitled "Nano-Innov" [**26**] and the second FINMINA, for Innovating in the Teaching of Microelectronics and Nanotechnologies [**27-29**], as part of the French government's Excellence Initiative [**30**] multi-year program.

These two national innovation programs have provided financial support to develop innovative practice training on the platforms of the national network. These practice trainings are directly linked to the skills and competences of the teaching teams and thus with the research laboratories. A selection of practices is made by the Council of the network in order to be compatible with the facilities of the CNFM centers. In average, more than fifteen innovative subjects of practice training are proposed in the catalog of each center. After 8 years of applying this strategy, several thousand students can acquire each year a know-how in nanoelectronics and

nanotechnology. We detail below several subjects that appear the more significant for our purpose.

Innovative practice developed in several CNFM centers

In this section, several examples are given on the practice developed by the CNFM centers involved in nanotechnologies education. There are sorted in subsections with a title giving the main topics and the CNFM centers concerned.

Graphene based devices at CNFM center of Lille

Graphene appears to be a promising material due to its very high conductive properties. Much work has been done to create very small devices with low energy consumption and relatively high driving current [**31**]. This material in a single-layer atomic configuration can form the channel region of a MOSFET transistor as shown in **Fig. 10**.

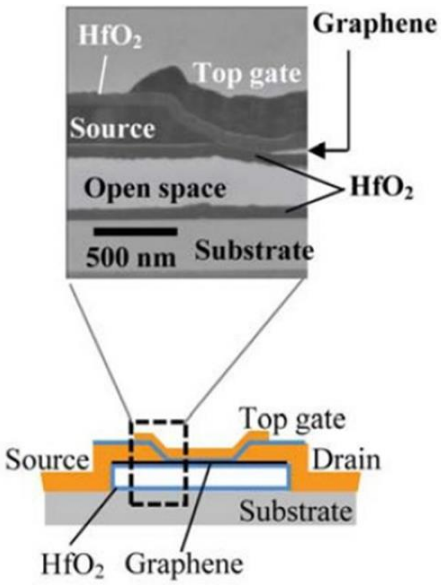

Fig. 10. Graphene based transistor fabricated in the CNFM center of Lille. This practice training results of research activities performed at the IEMN laboratory [31].

Metal/Insulator/Metal architectures at CNFM center of Grenoble

Based on the research activities of the LTM laboratory in Grenoble (Laboratoire des Technologies de la Microélectronique), several studies on the stacking of very thin layers of metal/insulator/metal have been published [**22**] in order to develop new integrated memories at the nanometric scale. The first structure concerns OxRAM (Oxide based Random Access Memory) fro which the principle was published in 2012 [**32**], based on the stacking of metal-insulator-metal layers. This structure is intended for an application "Above IC" [**2**], as shown in **Fig. 11(a)**.

In this case, the students discover the way to grow very thin films with a specific technique, the Atomic Layer Deposition (ALD) that is processed close to the room temperature, as shown **Fig. 11(b)**. This process is very well adapted to heterogeneous technologies by avoiding the effects of the high temperature technological steps, more especially on the physical transformation of the materials and on the diffusion of species (doping atoms for example) in the pre-existing layers and zones.

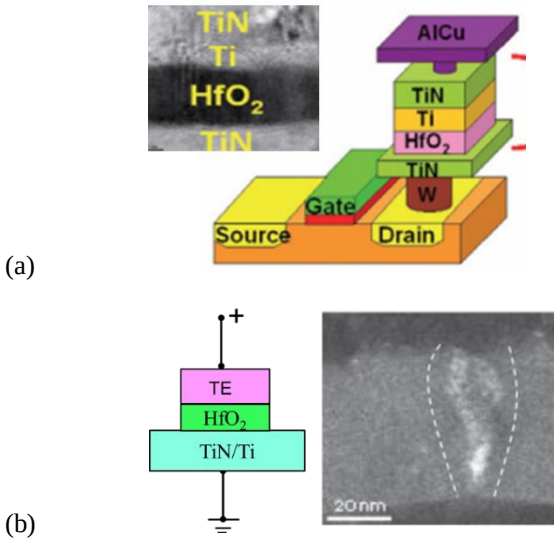

Fig. 11. OxRAM (Oxide based Random Access Memory) based on the stacking of Metal-Insulator-Metal (a). The students have fabricated the stacked layers in cleanroom and characterized the thin oxide of Hafnium to detect the percolation of the layer (b) [22].

Another structure developed in the same center is a Metal-Insulator-Metal (MIM) capacitance memory as shown **Fig. 12**. This MIM memory is involved in a three-dimension architecture that allows increasing significantly the area of the device and thus the efficiency of the memory. Deep trenches are filled through successive atomic layer depositions (ALD) of TiO_2, RuO_2 and Ru [**32**]. In order to give to the students some know-how on the ALD deposition technique, a training was built consisting to realize a planar structure that is much easier to process (Fig. 12 right) and that is physically and electrically characterized.

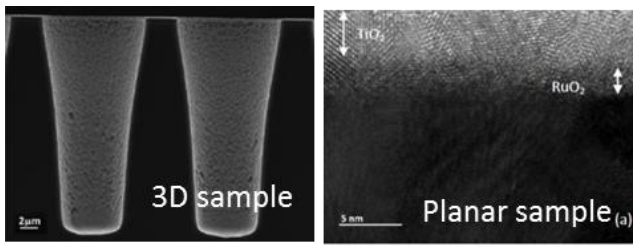

Fig. 12. Left: Metal-Insulator-Metal structure ($Ru/RuO_2/ATO/Pt$) issued from research activities. Deep trenches are filled through successive atomic layer depositions of TiO_2, RuO_2 and Ru. Right: layers that are grown by ALD by students in a planar configuration in order to simplify the fabrication process [22,32].

This training enables students to work in clean rooms and analyze the microstructure of films.

Silicon nanowire based transistors

Silicon nanowires are considered a possible way to further reduce the size of elementary devices according to Moore's law. **Fig. 12** shows the principle of the nanowire-based transistor proposed by Chuan Wang *et al*. [**33**]. This type of structure was first developed and manufactured in the IETR laboratory [**34**]. Subsequently, the process was transferred for educational purposes [**35**].

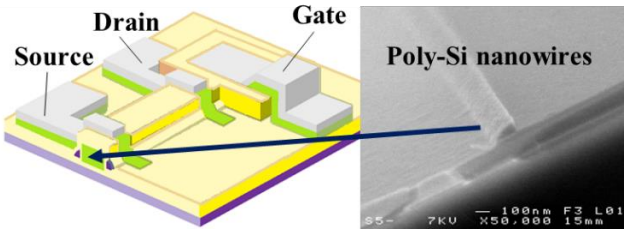

Fig. 12. Silicon nanowires based transistor developed at IETR. This structure is proposed in the catalog of the practice training. The students can fabricate the device [**35**].

This fabrication includes the manipulation of the nanowires in a dedicated chamber with a nanorobot thanks to an Atomic Force Microscope (AFM) [**36**], as shown **Fig. 13**.

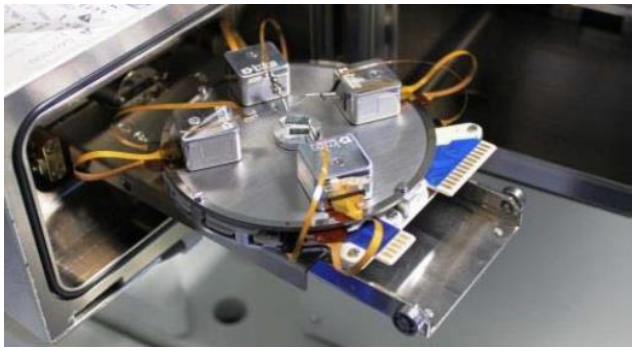

Fig. 13. Nanorobot for manipulation of nanowires in the cleanroom of CNFM center of Rennes. [**36**].

Fig. 14 shows a picture of the devices fabricated by the students. In this case, the nanowires are used as sensors [**36**]. Several nanowires are suspended, a way to improve the sensitivity of the detector.

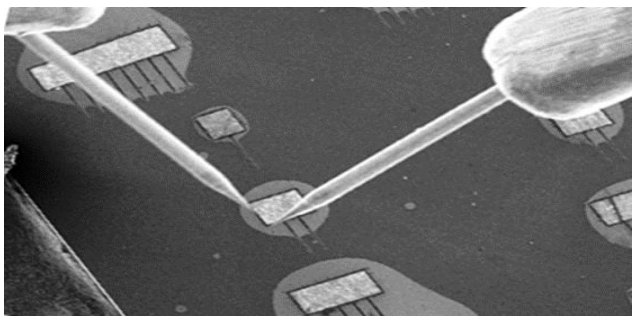

Fig. 14. Example of manipulation of nanowires by students with the nanorobot [36].

The students have thus acquired a know-how at the level of the nanometer, with associated electrical characterizations.

Nanocrystals inside at the CNFM center of Toulouse

Nanocrystals have specific properties due to quantum confinement. A silicon nanocrystal within a polysilicon gate of a MOS transistor can act as a localized trapping zone with a nanometric size and give charge storage properties within the insulating gate [**37**]. This is a way of manufacturing and controlling integrated memories. Resulting from research activities, students have access to the realization of such a structure at the CNFM center in Toulouse [**38**].

Fig. 15 shows the principle of memory in an inset and the microscopic observation of nanocrystals in the gate of a transistor fabricated at the CNFM center in Toulouse.

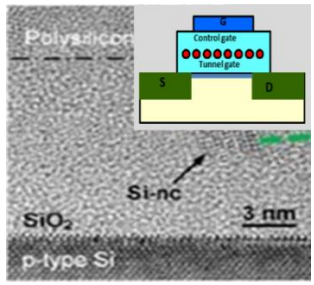

Fig. 15. "Nanocrystals Inside" or nanodots in integrated memories. This structure developed by the CNFM center of Toulouse was proposed to master and engineer students [38].

This practice gives the opportunity to the students to highlight some effects that occur at the nanometric dimension.

Carbon nanotubes inside transistors at CNFM Paris-Sud center

As with graphene studies, carbon nanotubes appear to be a good candidate for ULSI (Ultra Large Scale Integration) due to the good transport properties of this material. Many studies have been carried out for more than fifteen years on these nanotubes [**39**]. The potential applications are very similar to those of silicon nanowires, with the nanotubes positioned between two contacts that act as the source and drain of a transistor.

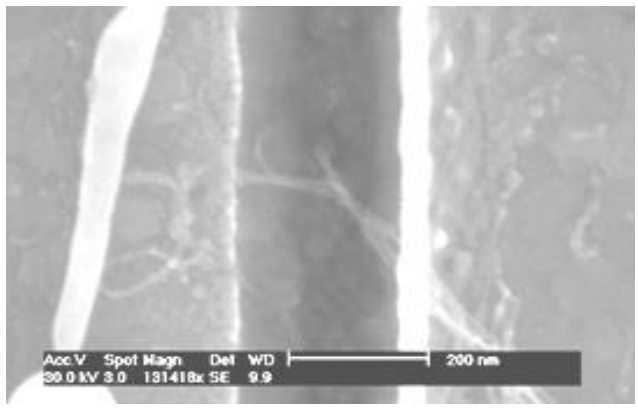

Fig. 16. Carbon nanotube in integrated memories. Nanotube is positioned between two Aluminum electrodes [39]. This structure was developed by researchers of C2N laboratory [40] and transferred to the cleanroom of the CNFM center of Paris-Sud.

Giant magneto resistance structure (GMR) at CNFM center of Paris-Sud

Giant magnetoresistance (GMR) is a quantum mechanical magnetoresistance effect observed in thin film structures composed of alternating ferromagnetic and nonmagnetic layers [**41**], first developed at Paris-Sud University, and was the matter of a Nobel Prize obtained by A. Fert and P. Grünberg in 1988. The effect manifests itself as a significant decrease in electrical resistance in the presence of a magnetic field. This effect can be used in the fabrication of hard disks. This research was transferred to the CNFM center of Paris-Sud. **Fig. 17** shows a top view of a GMR device fabricated and characterized by students.

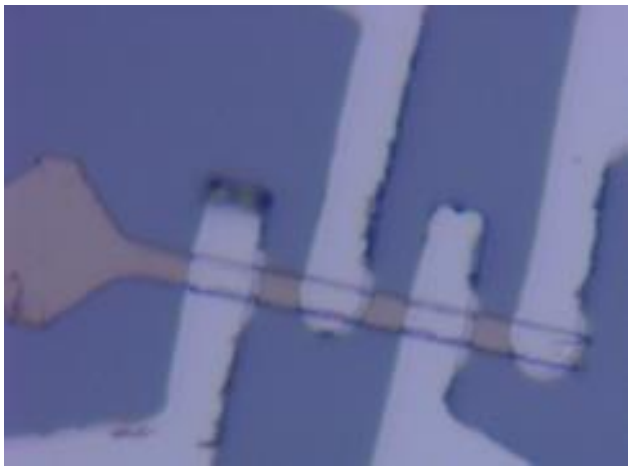

Fig. 17. Giant Magneto-Resistance (GMR). Based on a structure ferro/non-magnetic/ferro (FeCo/Cu/NiFe) [41], designed and fabricated at the CNFM center of Paris-Sud.

The fabrication and analysis of both types of devices has allowed students of the CNFM center of Paris-Sud to be at the heart of nanotechnology research, a way to motivate themselves to pursue studies in this field.

Design of integrated circuits in nanoscale technologies at CNFM Grenoble center

Integrated processes have already reached the nanoscale for the minimum size of elementary devices, most of them being MOS transistors in FDSOI (Fully depleted Silicon on Insulator devices) or FinFET (Fin Field Effect Transistor) architectures, these two main technologies being already in production. Students must have knowledge of the design of these technologies [**42**]. Several practical training courses have been set up allowing some students to design specific circuits in these modern manufacturing processes. Figure 18 shows a design carried out by a group of students with the CNFM center in Grenoble, in this case a finite impulse response FIR filter.

In addition, as part of an internship, students also have the opportunity to physically fabricate a prototype using the Multi Chip Project service (French CMP) and test their own circuits. It is a way to become familiar with industrial nanometric technologies.

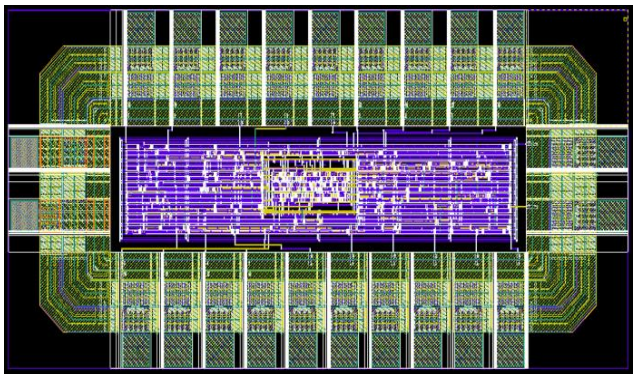

Fig. 18. Design of an integrated circuit (FIR filter) in the new nanometric technologies [42].

Conclusion and future perspectives

In summary, this article does not provide the latest research results, but presents how to maintain a high scientific level and skills based on the knowledge and know-how of future engineers and researchers, which is a real challenge today. We have given several examples of research studies conducted in the field of nanoelectronics and nanotechnologies that have led to the creation of several practical training courses on dedicated platforms capable of raising awareness among students and future engineers, and even doctors. It may be assumed that nanotechnologies have not yet clearly reached the market, but developments in connected objects and the Internet of Things are increasingly including nano-elements, nano-devices and nano-technologies. In addition, it has been shown that the pooling of equipment and the functioning of dedicated platforms, applied as part of the national strategy in France, is the most effective way to develop training. This strategy can be disseminated to other countries. This should ensure the fabulous evolution of connected objects in the expected digital society!

Acknowledgment

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Keywords

Nanoelectronics, nanotechnologies, higher education, pedagogy, French national network.

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